REMARKS/ARGUMENTS

1. Rejection of claims 1-5, 7-12, 14 and 15 as being anticipated by Schadt et al. (US Patent 6,870,395):

Claim 1:

Claim 1 has been amended to overcome this rejection. Specifically, the limitations "each sub-circuit cell comprising at least two types of sub-circuit blocks" and "each layout in the connection layer corresponding to each sub-circuit cell is selectively connected to the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions" have been added to claim 1. This amendment finds support in original claim 4, in paragraph [0022] in the specification and in Fig. 3, and no new matter is introduced. For instance, in paragraph [0022] and in Fig. 3, a plurality of different types of sub-circuit blocks B1 to B6, which can realize different I/O functions, are disclosed.

Compared to US 6,870,395, the applicant believes the amended claim 1 is patentably distinct, and explains as follows:

In the present application, each sub-circuit cell comprises *at least* **two types of sub-circuit blocks**, and different circuit functions are implemented by selectively connecting or not connecting *the sub-circuit blocks in each sub-circuit cell* when performing the layout programming in the connection layer. In Schadt's teaching, he does not teach using different types of SLBs, and different functions are implemented by using the connectivity structure to *connect each SLB to other units e.g. I/O buffer, PLC, or memory blocks*. The applicant quotes the SLB signal connectivity portion (col. 4, line 41-col. 5, line 26) of Schadt's teaching as follows:

"PLD 200 of FIG. 2 utilizes two connectivity structures to integrate the standard-cell gates of each SLB 220 with the rest of the device. The first connectivity structure is a perimeter-based structure that runs, e.g., over the I/O circuitry on an upper layer of

metalization. This perimeter-based connectivity structure programmably connects **each SLB to either I/O buffers, the programmable logic core, or both**. The second connectivity structure is a core-based structure that runs, e.g., over the block memory on upper layers of metal. This core-based connectivity structure programmably connects **each SLB to either memory blocks, the programmable logic core, or both**. The regions of metal layers used in PLD 200 for these two connectivity structures correspond to regions of metal layers that are underutilized in typical FPGAs, such as FPGA 100 of FIG. 1.

FIG. 3 shows a block diagram representing the possible interconnections between a particular SLB 220 in PLD 200 of FIG. 2 and one or more I/O buffers 210, one or more PLBs 206, and one or more memory blocks 208, according to one embodiment of the present invention. As shown in FIG. 3, switch box 302 (e.g., a set of muxes) provides programmable connectivity via routing resources 304 between SLB 220, logic blocks 206, and muxes/demuxes 212 corresponding to I/O buffers 210. **Switch box 302 and routing resources 304 form part of the first, perimeter-based connectivity structure of PLD 200**. Similarly, switch box 306 (e.g., another set of muxes) provides programmable connectivity via routing resources 308 between SLB 220, logic blocks 206, and memory blocks 208. **Switch box 306 and routing resources 308 form part of the second, core-based connectivity structure of PLD 200**.

The **muxes** in switch boxes 302 and 306 are independently programmable to provide flexible connectivity between the various elements of PLD 200. **In particular**, switch boxes 302 and 306 can be programmed via software control to provide signal flow in a variety of ways between SLB 220 and the rest of PLD 200. Significantly, switch boxes 302 and 306 can also be programmed to bypass SLB 220 completely. According to this programmable configuration, switch box 302 is configured to provide connections between I/O buffers 210 and PLBs 206, while switch box 306 is configured to provide connections between memory blocks 208 and PLBs 206, with no connections provided to SLB 220. Note that, when configured with all of the SLBs 220 bypassed, PLD 200 will operate as a conventional FPGA.

In one possible implementation, each SLB 220 is connected to the rest of PLD 200 by 1,810 wires, which number should be sufficient for SLBs ranging from 5K to 500K gates. In other implementations, other numbers of wires can be used, including a single PLD having multiple SLBs, each with a different number of wires, e.g., depending on the size and/or functionality of the SLB."

It can be seen from Schadt's teaching that the connectivity structure is used to connect the SLB to other units of the PLD, but not to provide connection between SLBs. For instance, the perimeter-based connectivity structure is used to programmably connect each SLB to either I/O buffers , the programmable logic core, or both. The core-based structure is used to programmably connect each SLB to either memory blocks, the programmable logic core, or both.

In addition, Schadt teaches that the switch box 302 and routing resources 304 form part of the perimeter-based connectivity structure of PLD 200 (col. 4, lines 65-66), and that the switch box 306 and routing resources 308 from part of the core-based connectivity structure of PLD 200 (col. 5, lines 3-5). This indicates that Schadt's connectivity structure is not simply a physical wiring. Since the connectivity structure includes switch box 302, 306, the programmable connection between different units of PLD has to be achieved **by muxes via software control**.

In summary, there are two main differences between the present application and Schadt's teaching. First, the method of the present application programmably connects different types of sub-circuit blocks in the same sub-circuit to achieve different circuit functions, while Schadt's method requires to connect the SLBs to other portion of the PLD e.g. I/O buffers or memory blocks. Second, the programming of the present application is achieved only by changing the layout of the connection layer. On the other hand, Schadt's method requires using muxes and software control to implement different circuit functions.

For the above reasons, claim 1 should be patentably distinct from the cited art.

Reconsideration of claim 1 is politely requested.

Claims 2-5, 7-8:

Claim 4 has been cancelled. Claims 2-3, 5, 7-8 are dependent upon claim 1, and should be allowable if claim 1 is found allowable. Reconsideration of claims 2-3, 5, 7-8 is politely requested.

Claim 9:

Claim 9 has been amended to overcome this rejection. Specifically, the limitations "each sub-circuit cell comprises at least two types of sub-circuit blocks" and "each layout of the connection layer selectively connects the sub-circuit blocks of each corresponding sub-circuit cell" have been added to claim 9. This amendment finds support in original claim 11, in paragraph [0022] in the specification and in Fig. 3, for instance. No new matter is introduced.

Claim 9 also includes the limitations distinct from US 6,870,395, and reconsideration of claim 9 is therefore requested in view of the aforementioned argument made to claim 1.

Claims 10-12, 14-15:

Claim 11 has been cancelled. Claims 10, 12, 14-15 are dependent upon claim 9, and should be allowable if claim 9 is found allowable. Reconsideration of claims 10, 12, 14-15 is politely requested.

2. Allowable Subject Matter:

Claim 6:

Claim 6 should not be objected and should be allowed if claim 1 is found

allowable.

Claim 13:

Claim 13 should not be objected and should be allowed if claim 9 is found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)